

SKY74068-21: Dual-Band Transmitter for CDMA and PCS Femtocell Applications

Applications

- Dual-band femtocells

Features

- Low power consumption in all operating modes
- Direct upconversion architecture
- Device controlled using a three-wire read/write serial bus interface with independent supply voltage
- Baseband RC filter to reject receive band noise
- Fully integrated VCO with auto-tuning
- Dual-mode fractional-N/integer-N PLL
- Variable gain PA drivers
- Differential cellular driver output matched to 200 Ω
- Single-ended PCS driver output matched to 50 Ω
- Transmit power control with >75 dB dynamic range
- Low current consumption at low transmit power minimizes current consumption and noise
- Hardware TX_ENABLE for gated mode operation
- RFLGA™ (32-pin, 5 x 5 x 1 mm) package with downset paddle (MSL3, 260 °C per JEDEC J-STD-020)

NEW

Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances) compliant packaging.



Description

The SKY74068-21 transmitter is a highly integrated device for dual-band Code Division Multiple Access (CDMA) femtocells. The SKY74068-21 supports femtocells in the cellular CDMA and Personal Communications System (PCS) modes.

The device requires a minimum number of external components to complete a CDMA radio subsystem. Included on-chip are the baseband filter, direct upconversion In-Phase and Quadrature (I/Q) mixers, variable gain power amplifier (PA) drivers, a fully integrated Voltage Controlled Oscillator (VCO) with Local Oscillator (LO) generation blocks, and a dual-mode fractional-N/integer-N Phase Locked Loop (PLL).

External components needed for operation include bias resistors, bypass capacitors, and passives to comprise the PLL loop filter.

The signal enters the chip as an analog baseband I/Q signal. It is filtered by the baseband filter and upconverted to the desired RF transmit frequency. The signal is amplified by one of two upconverters, depending on whether the chip is operating in cellular or PCS mode. The resulting signal is fed through the appropriate PA driver stage to provide variable output power and to drive the external PA. The signal is then filtered by an external Surface Acoustic Wave (SAW) filter and sent to the PA to obtain the final rated power.

The 32-pin RF Land Grid Array (RFLGA) device package and pinout are shown in Figure 1. Figure 2 shows a functional block diagram for the SKY74068-21.

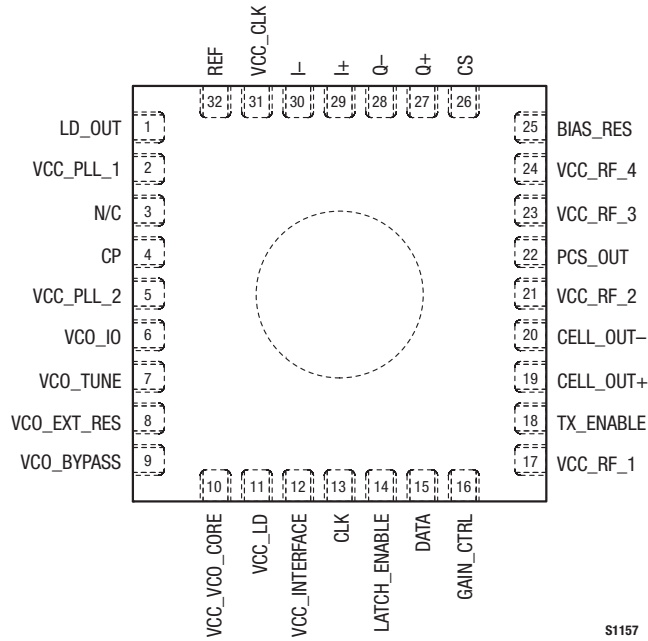


Figure 1. SKY74068-21 Transmitter Pinout – 32-Pin RFLGA (5 x 5 mm) (Top View)

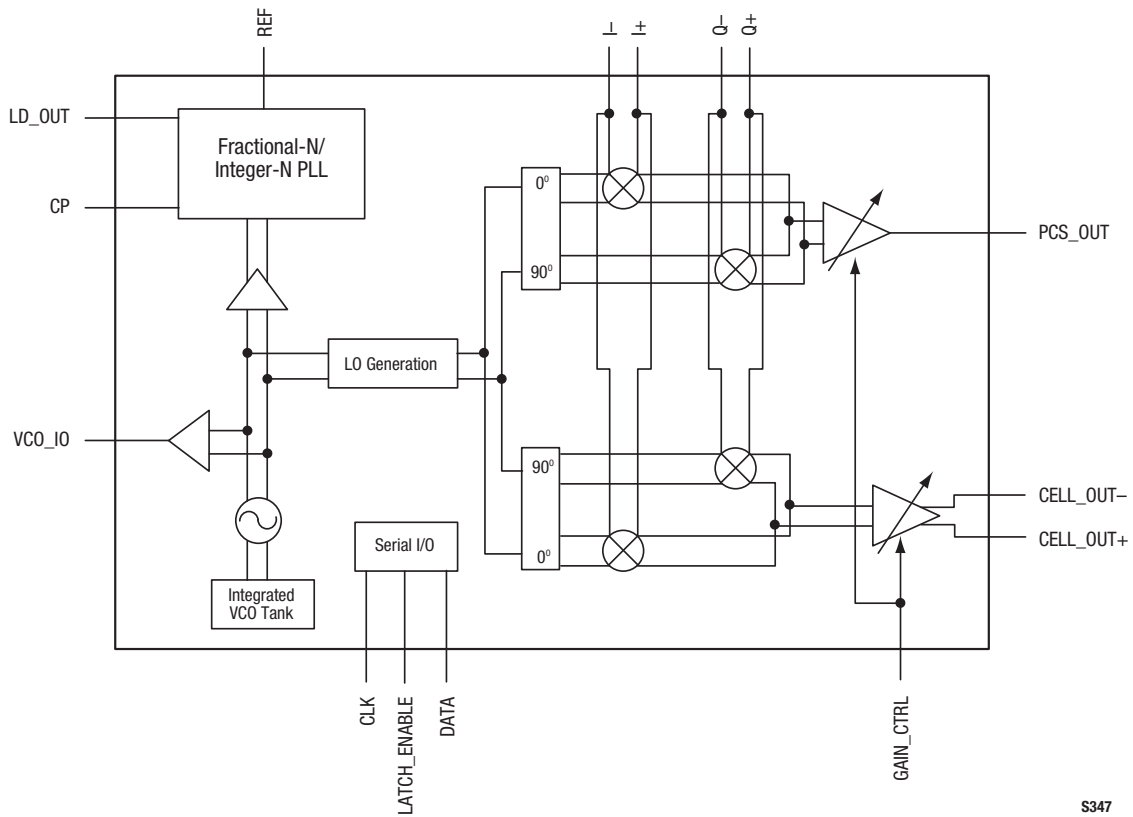


Figure 2. SKY74068-21 Transmitter Block Diagram

Technical Description

Baseband Filter

The SKY74068-21 has two modes of operation: current and voltage. In current mode, the device consists of a low resistive input. Together with an external capacitor across the differential inputs, the low resistive input acts as a low-pass filter.

In voltage mode operation, the baseband section of the SKY74068-21 contains a simple RC filter to reject receive band noise from incoming I and Q signals.

VCO, LO Chain, and PLL

The VCO has an internal tank circuit automatically tuned to the desired frequency. The VCO is connected to an on-chip PLL and LO generation blocks. The output of the LO generation blocks drives the LO port of the I/Q RF upconverter.

A dual-mode fractional-N/integer-N PLL is used to lock the VCO to the desired frequency in CDMA mode. A bi-directional buffer is available to measure the VCO output or to enable use of an external LO for testing purposes.

I/Q RF Upconverter

The I/Q RF upconverter converts the incoming I/Q signal to the desired RF output signal. The upconverter passes the output signal directly to the variable gain PA drivers. The LO for the upconverter is provided by the VCO and LO generation blocks.

The upconverter block consists of two separate mixers, one for cellular mode operation and the other for PCS mode. The output of the PCS mixer is routed to the PCS PA driver and the cellular mixer output is routed to the cellular PA driver.

Variable Gain PA Drivers

The SKY74068-21 includes two PA drivers. These drivers control the power level of the signal provided by the PCS and cellular upconverters. The gain of both drivers is variable, yielding over 75 dB of dynamic range.

The PCS driver output is single-ended, while the cellular driver is differential. Both are open collector outputs that require external matching.

Serial Bus Interface

A three-wire serial bus with read/write capability provides mode and bias control, and control of the PLL. The serial interface consists of three signals: a bus clock (CLK), a bus enable (LATCH_ENABLE), and the serial, bi-directional data line (DATA).

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY74068-21 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design & SMT Assembly/Rework Guidelines for RFLGA Packages*, document number 103147.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SKY74068-21 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

An application schematic diagram for the SKY74068-21 is shown in Figure 3. The package dimensions for the 32-pin RFLGA are shown in Figure 4, and the tape and reel dimensions are provided in Figure 5.

Table 1. SKY74068-21 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	LD_OUT	Lock detect output. Open drain.	17	VCC_RF_1	Supply for bias circuits of all drivers.
2	VCC_PLL_1	Supply for the PLL.	18	TX_ENABLE	Transmit enable/disable pin for all blocks, excluding VCO and PLLs.
3	N/C	No connection	19	CELL_OUT+	Positive cellular driver differential output.
4	CP	Charge pump output.	20	CELL_OUT-	Negative cellular driver differential output.
5	VCC_PLL_2	Supply for the PLL.	21	VCC_RF_2	Supply for PCS and cellular output drivers.
6	VCO_IO	Input/output port for the VCO bi-directional buffer.	22	PCS_OUT	PCS driver output.
7	VCO_TUNE	Loop filter input for the VCO.	23	VCC_RF_3	Supply for bias circuits of the PCS differential driver.
8	VCO_EXT_RES	External bias-setting resistor for the VCO.	24	VCC_RF_4	Supply for the mixer and associated bias blocks.
9	VCO_BYPASS	External capacitor for VCO noise filtering.	25	BIAS_RES	External bias resistor for all blocks, excluding VCO.
10	VCC_VCO_CORE	Supply for the VCO.	26	CS	Current sink.
11	VCC_LO	Supply for LO generation blocks.	27	Q+	Positive quadrature analog baseband input.
12	VCC_INTERFACE	Supply for serial bus.	28	Q-	Negative quadrature analog baseband input.
13	CLK	Clock signal for serial bus.	29	I+	Positive in-phase analog baseband input.
14	LATCH_ENABLE	Latch enable signal for serial bus.	30	I-	Negative in-phase analog baseband input.
15	DATA	Data signal for serial bus.	31	VCC_CLK	Supply for the TCXO buffer.
16	GAIN_CTRL	Gain control voltage.	32	REF	TCXO input.

Table 2. SKY74068-21 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage (VCC)		-0.3		+3.6	V
Input voltage range		-0.3		VCC	V
Storage temperature		-40		+125	°C
Ambient operating temperature		-30		+85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SKY74068-21 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage		2.70	2.85	3.00	V
Logic level: high low		VCC – 0.5 0		VCC 0.5	V V
Z _{IN} of logic control inputs			50		kΩ
Supply current: CDMA mode @ 5 dBm PCS mode @ 5 dBm			71 76		mA mA
Supply current in sleep mode				100	μA

Table 4. SKY74068-21 Electrical Specifications (Note 1) (1 of 3)
(T_A = +25 °C, VCC = 2.85 V, CDMA2000 Waveform Used Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Baseband Filter						
Cutoff frequency			3			MHz
Amplitude ripple				0.5		dB
Amplitude imbalance between I and Q chains				0.20	0.25	dB
Phase imbalance between I and Q chains				1		degrees
Rejection: @ 45 MHz (CDMA) @ 80 MHz (PCS)				20 25		dB dB
I/Q RF Upconverter, Voltage Mode						
Input signal level				1		Vp-p differential
Input common mode voltage			1.3	1.5	1.9	V
Input impedance				50		kΩ
I/Q Upconverter, Current Mode						
Input signal level				1 ± 0.6		mA
Current sink			20		200	μA
I/Q RF Upconverter and Driver, CDMA						
I/Q frequency range				0.63	2.5	MHz
–1 dB bandwidth				5		MHz
RF output frequency range			800	836	950	MHz
Maximum RF output power				+5		dBm
Dynamic range			75			dB
Control voltage range			0.2		2.7	V
Slope of RF AGC			30	50	75	dB/V
ACPR: 750 kHz offset @ +4 dBm 1.98 MHz offset @ +0 dBm				–55 –70		dBc dBc

Table 4. SKY74068-21 Electrical Specifications (Note 1) (2 of 3)
(T_A = +25 °C, V_{CC} = 2.85 V, CDMA2000 Waveform Used Unless Otherwise Noted)

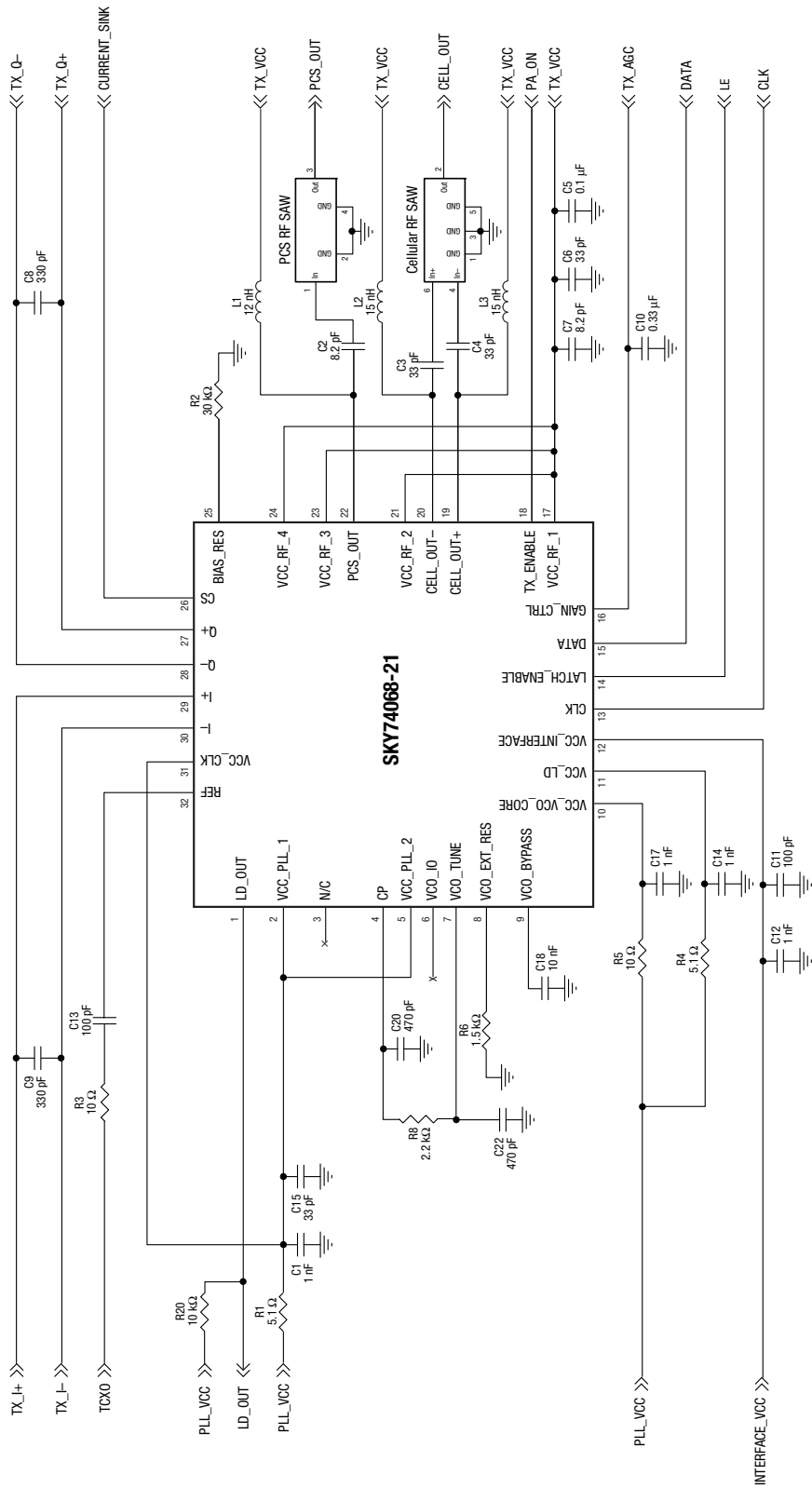
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
<i>I/Q RF Upconverter and Driver, CDMA (continued)</i>						
Residual sideband suppression				-38	-35	dBc
Carrier suppression (Note 2)				-35	-32	dBc
Gain variation over the frequency band		824 MHz to 849 MHz		0.5	1.0	dB
Output return loss @ maximum power				-12	-10	dB
Receive band noise @ maximum gain, P _o = +8 dBm				-137	-135	dBm/Hz
Noise floor @ minimum controlled output power = -81 dBm/1.23 MHz				-165	-160	dBm/Hz
Supply current including LO chain: Current mode @ minimum power				26	30	mA
Current mode @ -30 dBm				40	46	mA
Current mode @ +8 dBm				60	69	mA
Supply current including LO chain: Voltage mode @ minimum power				22	25	mA
Voltage mode @ -20 dBm				35	40	mA
Voltage mode @ +8 dBm				60	69	mA
Settling time for output power to reach ±1 dB of final value				5		µs
<i>I/Q RF Upconverter and Driver, PCS</i>						
I/Q frequency range				0.63	2.5	MHz
-1 dB bandwidth				5		MHz
RF output frequency range			1700	1880	2000	MHz
Maximum RF output power				+5		dBm
RF dynamic range			75			dB
Control voltage range			0.2		2.7	V
Slope of RF AGC			30	50	80	dB/V
ACPR: 885 kHz @ +1 dBm				-52		dBc
1.25 MHz offset @ +1 dBm				-55		dBc
1.98 MHz offset @ +2 dBm				-70		dBc
Residual sideband suppression				-35	-35	dBc
Carrier suppression (Note 2)				-35	-32	dBc
Output return loss @ maximum power				-12	-10	dB
Receive band noise @ maximum gain, P _o = +5 dBm				-134		dBm/Hz
Noise floor @ minimum controlled output power = -79 dBm/1.23 MHz				-165	-160	dBm/Hz

Table 4. SKY74068-21 Electrical Specifications (Note 1) (3 of 3)
(T_A = +25 °C, V_{CC} = 2.85 V, CDMA2000 Waveform Used Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
I/Q RF Upconverter and Driver, PCS (continued)						
Supply current including LO chain:						
Current mode @ minimum power				23	26	mA
Current mode @ -30 dBm				40	46	mA
Current mode @ +9 dBm				64	72	mA
Supply current including LO chain:						
Voltage mode @ minimum power				19	23	mA
Voltage mode @ -30 dBm				40	46	mA
Voltage mode @ +5 dBm				66	76	mA
Settling time for output power to reach ±1 dB of final value				5		µs
VCO/PLL in CDMA Mode						
Phase noise:						
@ 100 kHz offset				-100	-95	dBc/Hz
@ 885 kHz offset				-120	-110	dBc/Hz
@ 1.98 MHz offset				-130	-120	dBc/Hz
Total supply current				5.5		mA
Fractional-N PLL						
Reference range			1.0	19.2	40.0	MHz
Reference input sensitivity			200	500		mVp-p
Charge pump current, RF (sel 1)			0.032	0.040	0.048	mA
Charge pump current, RF (sel 2)			0.08	0.10	0.12	mA
Charge pump current, RF (sel 3)			0.16	0.20	0.24	mA
Charge pump current, RF (sel 4)			0.32	0.40	0.48	mA
Charge pump leakage current					0.10	nA
PLL phase noise integrated from 1 kHz to 630 kHz at carrier:		Unity gain loop bandwidth = 25 kHz				
CDMA (F _{comp} = 9.6 MHz)				2		degrees rms
PCS (F _{comp} = 9.6 MHz)				2		degrees rms
Supply current				4		mA
Integer-N PLL						
Input frequency minimum range			500		2500	MHz
Reference range			1.0	19.2	40.0	MHz
Phase detector frequency minimum range			10		1000	kHz
Reference input sensitivity			200	500		mVp-p
Charge pump current, RF (sel 1)			0.22	0.28	0.34	mA
Charge pump current, RF (sel 2)			0.56	0.70	0.84	mA
Charge pump current, RF (sel 3)			1.12	1.40	1.68	mA
Charge pump current, RF (sel 4)			2.24	2.80	3.36	mA
Charge pump output voltage compliance, minimum range			0.5		VDD - 0.5	V
Supply current				3.5		mA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

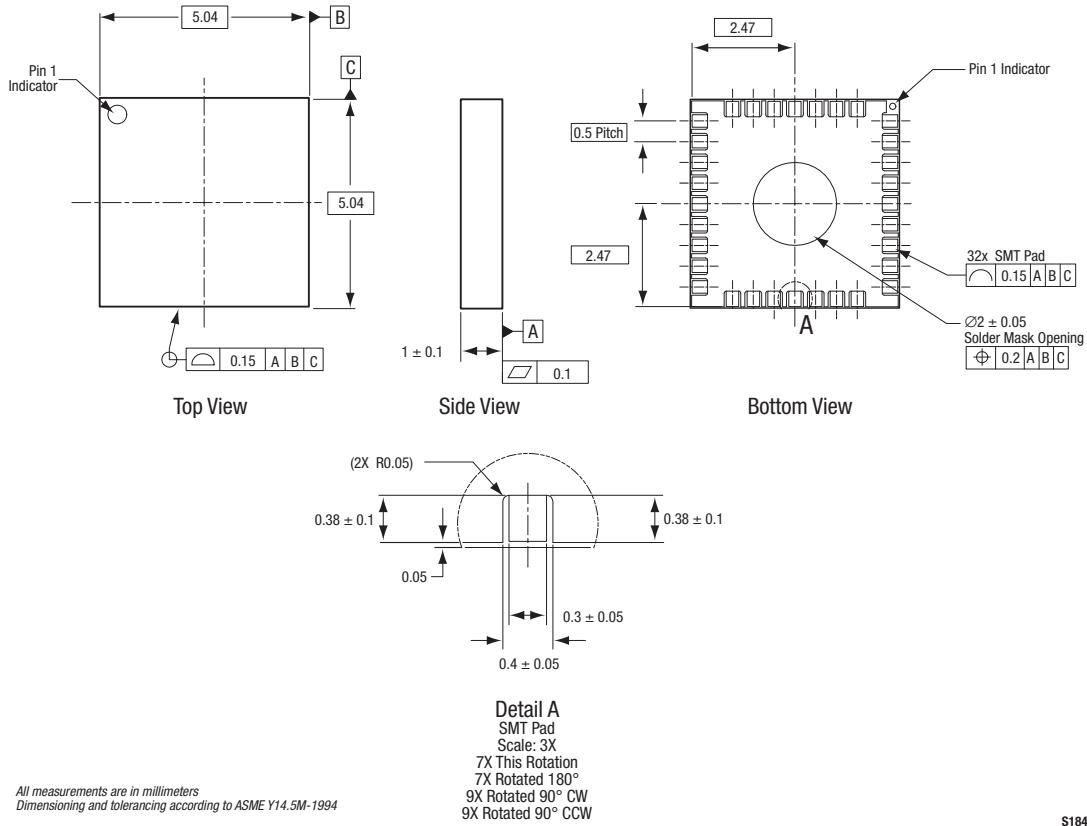
Note 2: Minimum of -20 dBc at minimum power.



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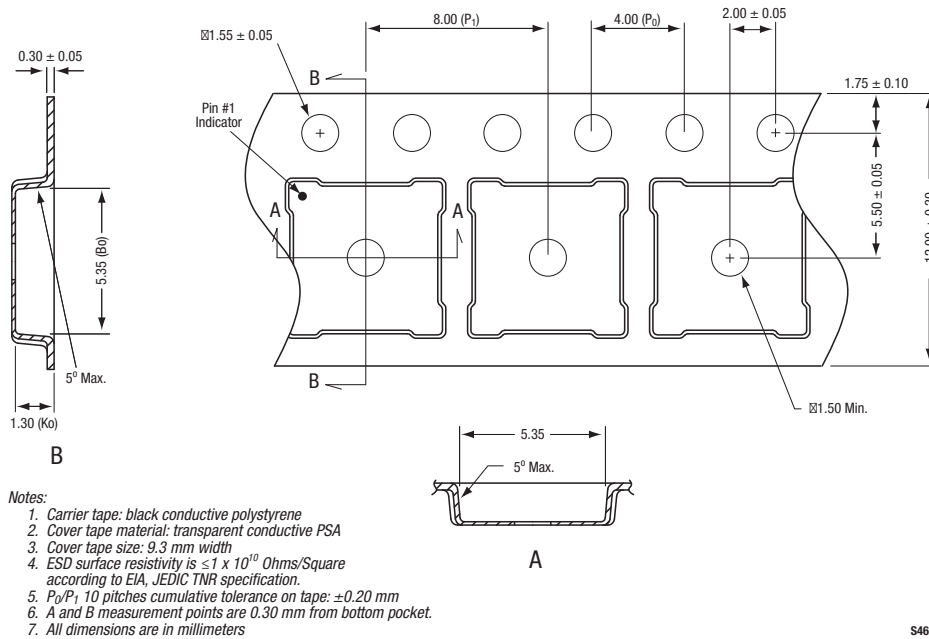
Note: Capacitors C8 and C9 are used only in the current operation mode.

Figure 3. SKY74068-21 Application Schematic



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Figure 4. SKY74068-21 32-Pin RFLGA Package Dimension Drawing



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Figure 5. SKY74068-21 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY74068-21 Transmitter	SKY74068-21	*** TBD ***

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